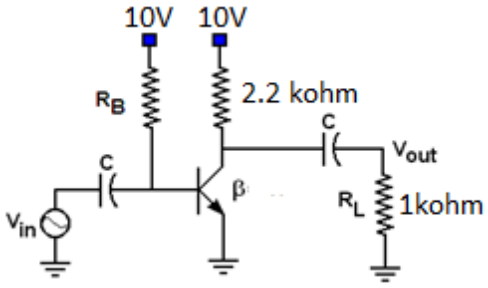
Electronics

Load lines in BJT amplifiers

Problem 1.- In the circuit shown below, the transistor's beta is 150.

a) Find the value of R_B so that V_{CE}=5V at the Q point.
b) Draw the load line in DC of the transistor indicating the operating point found in (a).
c) Superimpose the AC load line on the Q point.
d) Find graphically (or calculating) the maximum amplitude that the voltage can oscillate in the load.



Solution: We first analyze the circuit in DC with the capacitors open. In the collector-emitter branch we have this equation

$$10V = 2.2k\Omega I_C + V_{CE}$$

Since the collector-emitter voltage is 5V, we can find the collector current as follows

$$I_C = \frac{10V - 5V}{2.2k\Omega} = 2.27mA$$

And with the given value of beta the base current is

$$I_B = \frac{I_C}{\beta} = \frac{2.27mA}{150} = 15.2\mu A$$

Then, we write the equation for the base side circuit to find the base resistance:

$$10V = R_B I_B + 0.7V \rightarrow R_B = \frac{10V - 0.7V}{I_B} = \frac{9.3V}{15.2\mu A} = 613k\Omega$$

To draw the load line we notice that the intercepts with the axes are 10V and a saturated current of

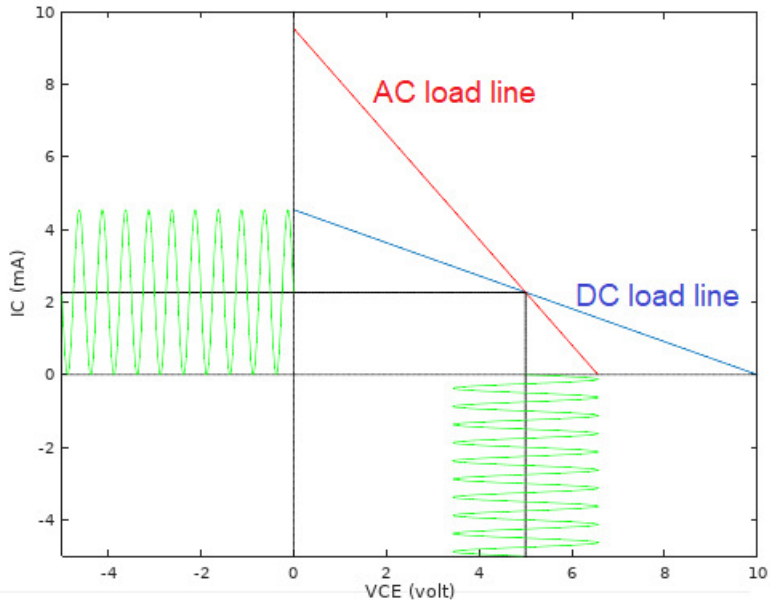
$$I_{saturation} = \frac{10V}{2.2k\Omega} = 4.55mA$$

The AC impedance is given by

$$2.2k\Omega // 1k\Omega = \frac{2.2k\Omega \times 1k\Omega}{2.2k\Omega + 1k\Omega} = 688\Omega$$

That means that the slope of the AC load line is $m = -\frac{1}{688\Omega}$

The graph is shown below

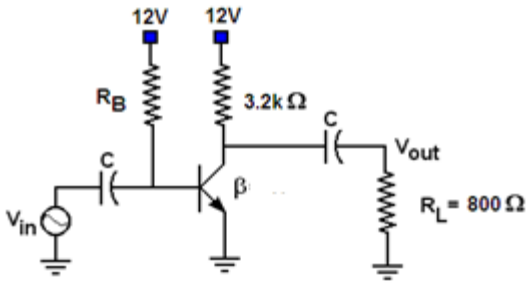


The maximum oscillation in the load can be obtained by looking at the limits of the AC load line. On the negative side we can reach -5V, but on the positive side we can only reach

$$V_{\max} = 2.27mA \times 688\Omega = 1.56V$$

If we want symmetric oscillations in the load (without distortion) we need to limit the amplitude to 1.56V

Problem 1a.- For the circuit shown in the figure beta is 100.
a) Find the value of R_B so that $V_{CE} = 6V$ at the Q point.
b) In these conditions find what is the maximum symmetric oscillation in the load. Assume that the capacitors behave as shorts in AC.



Solution.- The DC analysis gives us:

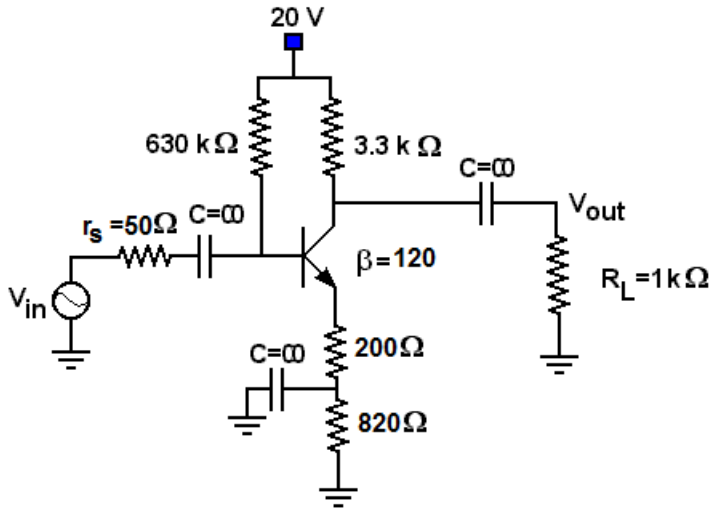
$$I_{CQ} = \frac{12V - 6V}{3.2k\Omega} = 1.88mA \text{, and } I_{BQ} = \frac{1.88mA}{100} = 18.8\mu A$$

Then $R_B = \frac{12V - 0.7V}{18.8\mu A} = 600k\Omega$

We notice that the output impedance is $R_C \,//\, R_L = \frac{800 \times 3.2k}{800 + 3.2k} = 640\Omega$

Given the position of the Q point and this impedance, the maximum amplitude of a symmetric oscillation is $\Delta V = 1.88mA \times 640\Omega = 1.2V$

Problem 2.- For the circuit shown below, draw its DC load line. Find the Q point and draw the AC load line that passes through it.



Solution.- The intercepts of the DC load line with the axes are 20V and

$$I_{SAT} = \frac{20}{3.3k + 200 + 820} = 4.63mA$$

The DC analysis gives us the Q point:

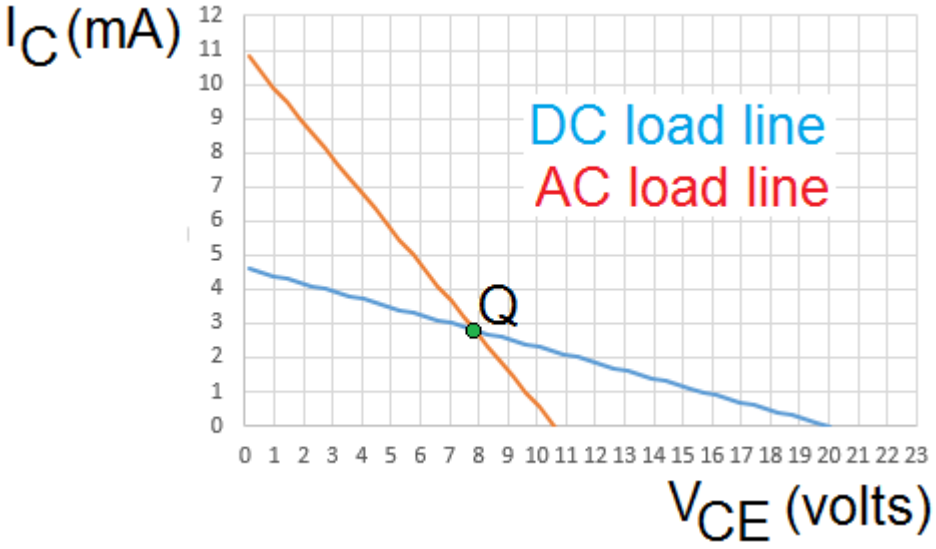
$$I_{BQ} = \frac{20 - 0.7}{630k + 120 \times (820 + 200)} = 25.6\mu A$$

$$I_{CQ} = 120 \times 25.6\mu A = 3.08mA$$

$$V_{CEQ} = 20V - 30.8mA \times (3.3k\Omega + 200\Omega + 820\Omega) = 6.70V$$

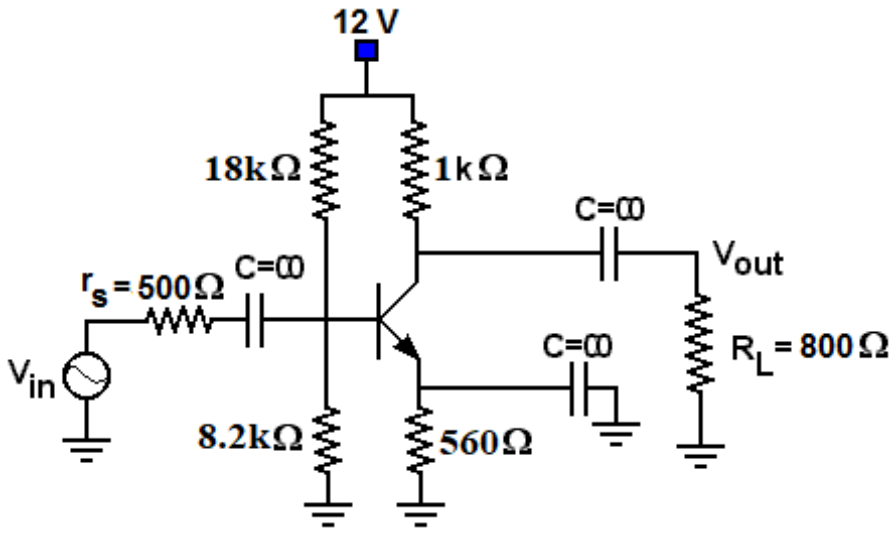
On this point we draw the AC load line with slope

$$-\frac{1}{3.3k \,//\, 1k + 200} = -\frac{1}{967\Omega}$$

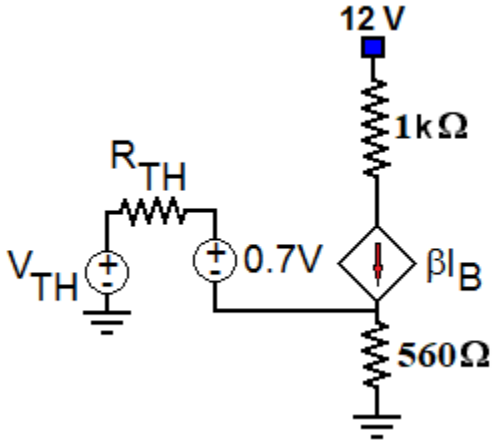


Problem 3.- For the amplifier shown below beta is 120.

a) What is the operating point V_{CE} and I_C?
b) What is the power in the transistor when there is no signal?
c) What is the impedance seen by the source v_{in} including r_s?
d) What is the output impedance of the amplifier?
e) Draw the DC load line indicating the Q point.
f) Superimpose the AC line on the Q point.
g) Calculate the maximum possible amplitude of a symmetric output.
h) Calculate the maximum v_{in} amplitude that does not saturate the transistor.



Solution:
a) In DC, the capacitors will behave as open circuits and the combination of resistors and 12V source can be replaced by a Thevenin equivalent as shown below.



With the values:

$$V_{TH} = 12\frac{8.2}{8.2+18} = 3.76V$$

$$R_{TH} = \frac{8.2\times 18}{8.2+18} = 5.63k\Omega$$

We can calculate the base current in DC.

$$I_B = \frac{3.76V - 0.7V}{5.63k\Omega + 0.56k\Omega\times 121} = 41.7\mu A$$

And find the operating point of the transistor.

$$I_C = \beta I_B = 120\times 41.7\mu A = 5.00mA$$

$$V_{CE} = 12V - 5mA(1k + 0.56k) = 4.19V$$

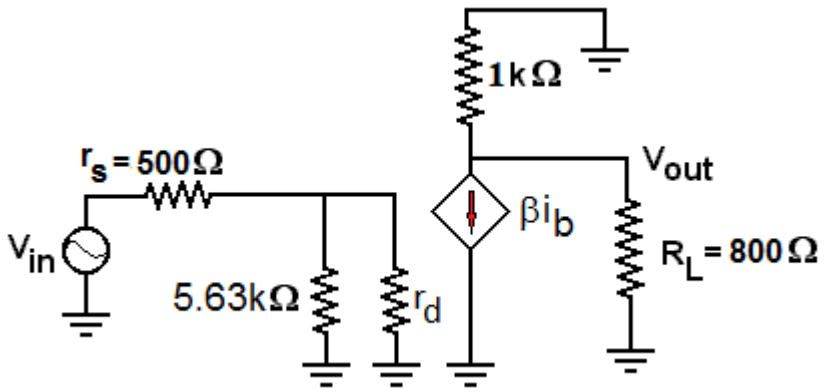
b) The power dissipated by the transistor at that point is

$$Pot = I_C V_{CE} + I_B V_{BE} = 5mA\times 4.19V + 0.7V\times 0.0417mA = 21mW$$

c) In AC, the emitter capacitor short-circuits the emitter resistance R_E. The base-emitter junction will behave as a dynamic resistance with a value:

$$r_d = \frac{26mV}{I_B} = \frac{26}{0.0417} = 624\Omega$$

The simplified circuit model becomes:



The input impedance is

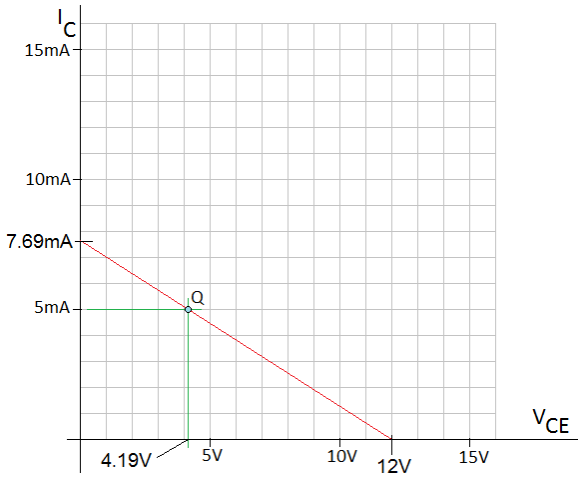
$$Z_i = r_S + r_d \,//\, R_{TH} = 500\Omega + \frac{624\Omega \times 5.63k\Omega}{624\Omega + 5.63k\Omega} = 1.06k\Omega$$

d) The output impedance is $Z_o = 1k\Omega$

e) The DC load line will have as limiting points:

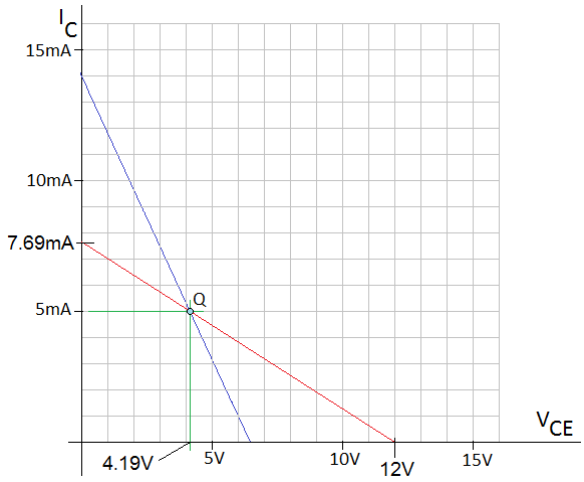
In cut-off $I_C = 0, V_{CE} = 12V$

In saturation $I_C = \frac{12}{1+0.56} = 7.69mA, V_{CE} = 0$



f) The AC load line will have a slope of $m = -\frac{1}{1k\Omega \,//\, 800\Omega} = -\frac{1}{444\Omega}$

Here we superimpose the AC load line on the graph.



g) The maximum symmetric amplitude is limited on the positive side, which is shorter. It can be calculated as:

$$V_p = 444\Omega \times 5mA = 2.22V$$

h) To find the maximum signal that can be amplified without distortion we take the voltage calculated above (2.22V) and divide it by the voltage gain.

To find the gain notice that the base current in AC is:

$$i_b = \frac{v_{in} \times 5.63k\Omega}{500\Omega + 5.63k\Omega} \frac{1}{5.63k\Omega // 500\Omega + 624\Omega} = 0.000848 v_{in}$$

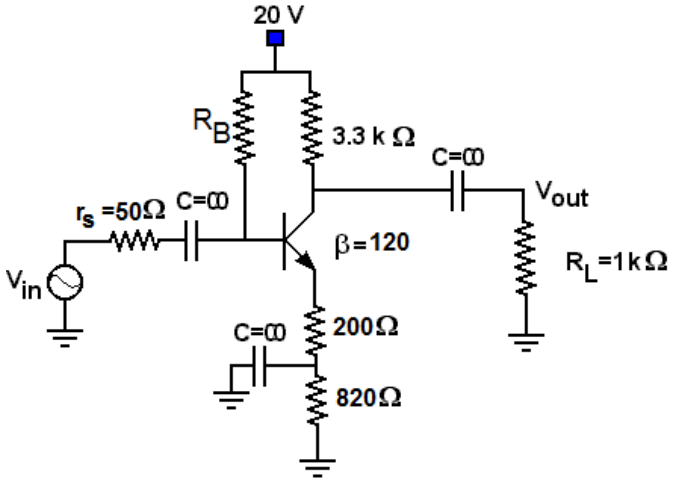
Then the collector current is $i_c = \beta i_b = 0.102 v_{in}$

And the output voltage $v_o = -i_c (1k\Omega // 800\Omega) = -45.2 v_{in}$

Since the gain is 45.2, the maximum amplitude that can be amplified without distortion is:

$$v_p = \frac{2.22V}{45.2} = 49.1mV$$

Problem 4.- For the circuit shown below, choose a value of R_B such that we can get the maximum possible symmetric oscillation in the collector current.
Show the DC and AC load lines in a graph.



Solution.- The extreme points of the DC load line are 20V and

$$I_{SAT} = \frac{20}{3.3k + 200 + 820} = 4.63mA, \quad \text{which gives us the equation } I_C = 4.63mA - \frac{V_{CE}}{4.32k\Omega}$$

On this line we will find the Q point and the AC load line, which will pass through it. The slope of the AC load line is

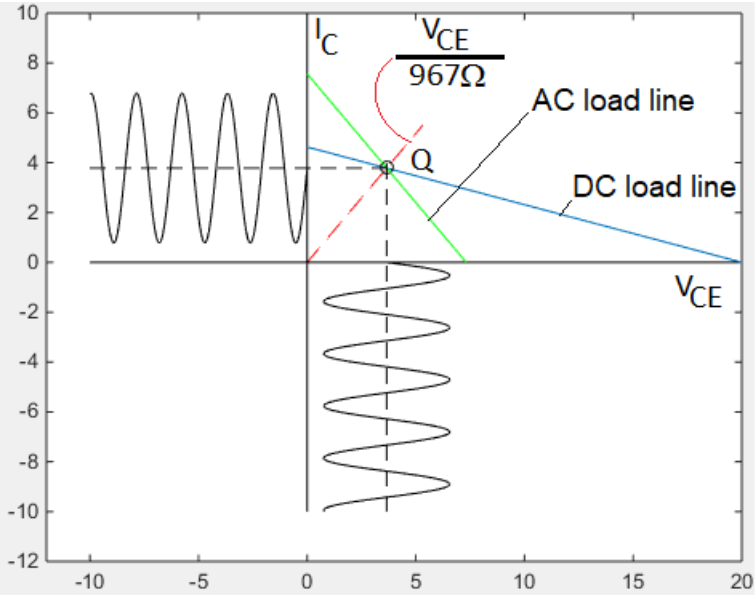
$$-\frac{1}{3.3k \,//\, 1k + 200} = -\frac{1}{967\Omega}$$

To obtain the maximum possible symmetric oscillation the Q point should be at the intersection of the DC load line with the auxiliary line

$$I_C = \frac{V_{CE}}{967\Omega}$$

This can be done graphically or analytically:

$$\frac{V_{CE}}{967\Omega} = 4.63mA - \frac{V_{CE}}{4.32k\Omega} \rightarrow V_{CE} = 3.66V \rightarrow I_C = 3.78mA$$



Analysis in DC gives us the R_B necessary to put the transistor in the desired Q point.

$$I_{BQ} = \frac{3.78mA}{120} = 31.5\mu A \qquad \rightarrow I_{BQ} = \frac{20 - 0.7}{R_B + 120 \times (820 + 200)} = 31.5\mu A \rightarrow R_B = 490k\Omega$$