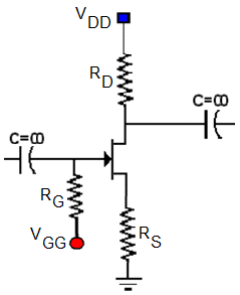
Electronics

J-FET biasing

Problem 1.- The J-FET based circuit shown below has the following specifications:

I_{DSS} = 12 mA, V_P = -6V, R_G = 1 MΩ, V_{GG} = -3V, R_D = 3.3 kΩ y R_S = 820Ω

1) Find the operating point of the transistor assuming it is in the active region.
2) Calculate the minimum value of V_{DD} to be in the active region.



Solution.- If the transistor is in the active region, the drain current is:

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$$

But because of the way it is biased, we notice that $V_{GS} = -3V - 820\Omega I_D$
That we can replace in the equation above to get:

$$I_D = 12mA\left(1-\frac{-3V-820I_D}{-6}\right)^2$$

Solving for I_D

$$36I_D = 12mA(3V - 0.82k\Omega I_D)^2$$

$$I_D = 1.27mA$$
$$I_D = 10.5mA$$

We accept the first solution as correct. The other (10.3mA) would make V_{GS} greater than V_P.

With this current we can now calculate the values at the Q point:

$$V_S = 1.27mA \times 0.82k\Omega = 1.04V$$
$$V_{GS} = V_G - V_S = -3V - 1.04V = -4.04V$$

The voltage drop in the drain resistor is:

$$V_{RD} = 1.27mA \times 3.3k\Omega = 4.20V$$

The minimum drain-source voltage is given by the relation between V_P and I_{DSS}:

$$V_{DS(\min)} = \frac{|V_P|}{I_{DSS}} I_D = \frac{6}{12}(1.27) = 0.63V$$

So the minimum source voltage has to be:

$$V_{DD(\min)} = 4.20V + 0.63V + 1.04V = 5.89V$$

With the understanding that a higher voltage would be better.